REMARKS/ARGUMENTS

The Examiner is thanked for the Office Action mailed May 10, 2007 and the courtesies extended during the telephone conference on August 7, 2007 regarding the IDS. The status of the application is as follows:

- Claims 1-26 are pending. Claims 1, 2, 6, 12, and 22 have been amended herein.
- The specification is objected to for informalities.
- Claims 1-9, 12-17, and 20-26 are rejected under 35 U.S.C. 102(b) as being anticipated by Noehring et al. (US Pub. 2002/0188839).
- Claims 10, 11, 18, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Noehring et al. in view of Trost et al. (US 4,627,018).

The objections and rejections are discussed below.

The IDS

The Office has indicated that the IDS filed October 4, 2004 fails to comply with 37 CFR 1.98(a)(3) as it does not include a concise explanation of the relevance, as it is presently understood by the individual designated in 37 CFR 1.56(c) most knowledgeable about the content of the information, of patents WO 99/14881 and JP9171500, which include English language Abstracts, but are not otherwise in the English language.

As suggested by the Examiner during the telephone conference of August 7, 2007, applicants submit that relevant portions of the patents WO 99/14881 and JP9171500 are the Abstracts, which are in the English language, and that an indication of the relevant portions of these patents was inadvertently omitted. Accordingly, Applicants respectfully request consideration of the Abstracts of the patents WO 99/14881 and JP9171500 by the Office during the pendency of the subject application.

The Specification

The Specification stands objected to for informalities. In particular, the Office notes that in the opening paragraph, referenced application serial numbers and filing dates are missing. A replacement paragraph has been submitted herein to cure these informalities. Accordingly, this objection should be withdrawn.

The Rejection of Claims 1-9, 12-17, and 20-26 under 35 U.S.C. 102(b)

Claims 1-9, 12-17, and 20-26 stand rejected under 35 U.S.C. 102(b) as being anticipated by Noehring et al. This rejection should be withdrawn because Noehring et al. does not teach each and every element as set forth in the subject claims.

> A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631 (Fed. Cir. 1987). MPEP §2131.

Claims 1, 2, 6, 12, and 22 have been amended herein. Applicants are not conceding in this application that claims 1, 2, 6, 12, and 22 are not patentable over the art cited, as the present claim amendments are only for facilitating expeditious prosecution. Applicants respectfully reserve the right to pursue these and other claims in one or more continuation and/or divisional patent applications.

Independent **claim 1** has been amended to include the aspects of claim 2 and now recites a system for secure data transfer over a network, including, *inter alia*, a network interface including a first data moving unit (DMU) configured to exchange secure data with a first portion of the network and a second DMU configured to exchange non-secure data with a second portion of the network. In the subject Office Action, the Office asserts that Noehring et al. discloses these claimed aspects. However, Noehring et al. does not teach or suggest such aspects.

More particularly, Noehring et al. relates to a method and system for high-speed processing IPSec security protocol packets. Noehring et al. discloses an ASIC 140 that is optimized for processing IPSec security protocol packets. The ASIC 140 includes an

input streaming interface 312 that receives IPSec packets from a Network Processor 130. When the entire packet is in external memory, portions are buffered in a local memory for crypto-processing. As portions of the packets complete processing, the portions are buffered to the external memory. When an entire packet completes processing, portions thereof are transmitted by an output streaming interface 326 of the ASIC 140 to the Network Processor 130. Hence, the input streaming interface 312 and the output streaming interface 326 of the ASIC 140 receive and transmit data to the Network Processor 130.

In the subject Office Action, the Office asserts that the combination of the Input FIFO & Context RAM 308 and the Input Crypto DMA Engine 310 of Noehring et al. teaches the first DMU. However, the Input FIFO & Context RAM 308 and the Input Crypto DMA Engine 310, individually and in combination, do not teach or suggest the first DMU. More particularly, claim 1 recites that the first DMU is configured to exchange secure data with a first portion of the network. As clearly shown in Fig. 3 of Noehring et al., both the Input FIFO & Context RAM 308 and the Input Crypto DMA Engine 310 are part of the Processing System 140 and neither exchanges data with any component or entity external to the Processing System 140, including the Network Processor 130.

Rather, the Input FIFO & Context RAM 308 receives data from an Input DMA Engine 306, which is also part of the Processing System 140; the Input FIFO & Context RAM 308 provides data to the Input FIFO & Context RAM 308; the Input Crypto DMA Engine 310 receives data from the Input FIFO & Context RAM 308; and the Input Crypto DMA Engine 310 provides data to a Crypto Core Engine 340, which is also part of the Processing System 150. As noted above, the Input FIFO & Context RAM 308 and the Input Crypto DMA Engine 310 are part of the Processing System 140 and neither exchanges data with any component or entity external to the Processing System 140, including the Network Processor 130. Thus, the combination of the Input FIFO & Context RAM 308 and the Input Crypto DMA Engine 310 does not teach or suggest the first DMU.

The Office also asserts that the combination of the Output Crypto FIFO 320 and the Output DMA Engine 322 Noehring et al. teaches the second DMU. However, the Output Crypto FIFO 320 and the Output DMA Engine 322, individually and in combination, do not teach or suggest the second DMU. More particularly, claim 1 recites that the second DMU is configured to exchange non-secure data with a second portion of the network. As clearly shown in Fig. 3 of Noehring et al., both the Output Crypto FIFO 320 and the Output DMA Engine 322 are part of the Processing System 140 and neither exchanges data with any component or entity external to the Processing System 140, including the Network Processor 130.

Rather, the Output Crypto FIFO 320 receives data from the Crypto Core Engine 340, which is also part of the Processing System 150 as discussed above; the Output Crypto FIFO 320 provides data to the Output DMA Engine 322; the Output DMA Engine 322 receives data from the Output Crypto FIFO 320; and the Output DMA Engine 322 provides data to an Output DMA Engine 324. As noted above, the Output Crypto FIFO 320 and the Output DMA Engine 322 are part of the Processing System 140 and neither exchanges data with any component or entity external to the Processing System 140, including the Network Processor 130. Thus, the combination of the Output Crypto FIFO 320 and the Output DMA Engine 322 does not teach or suggest the second DMU.

In view of the above, it is readily apparent that Noehring et al. does not teach each and every aspect as set forth in claim 1 and, thus, the rejection of claim 1 should be withdrawn.

Claim 2, which depends from claim 1, has been amended herein and recites that the first and second DMUs directly communicate with the first and second portions of the network. As noted above, the elements that the Office asserts teach the first and second DMUs are part of the Processing System 140 and do not communicate with any component or entity external to the Processing System 140. Thus, such elements of Noehring et al. cannot directly communicate with first and second portions of a network. As such, applicants request entry of this amendment and allowance of claim 2.

Claim 6, which depends from claim 5, recites that the logic configured to perform QoS operations includes, *inter alia*, logic configured to determine a priority of the

information flow, and logic configured to schedule at least one of the retrieving the portion of the data and the transferring of the operated-on portion of the data from memory based on the priority of the information flow associated with the portion of the data. **Claims 15 and 25** recite similar aspects.

The Office asserts that Noehring et al. teaches such claimed aspects at page 4, paragraph [0040]. However, this section of Noehring et al. does not teach or suggest the above claimed aspects. More particularly, page 4, paragraph [0040] describes the operation of the post-crypto packet processing system 146. As disclosed, the Output crypto FIFO 320 receives processed blocks of a security packet from the processing engine and the output DMA engine 322 transfers the processed blocks of the security packet to external output memory 158. The Rx DMA interface 324 retrieves the processed blocks from the memory 158 after all portions of the processed security data packet have been transferred to the memory 158. The Rx DMA interface 324 then transfers the processed blocks of the security data packet to a streaming interface for streaming.

The Rx DMA interface 324 preferably includes a plurality of registers storing length information each of a plurality of processed security data packets and retrieves the processed packets from the 158 in response to the storing of the length information for an associated processed security data packet. Hence, this section of Noehring et al. discloses storing data packet length information and retrieving the packet when its length information is stored. Thus, not only is Noehring et al. silent regarding storing priority information, but the retrieval of the packet is not based on the stored packet length information. Rather, the retrieval of the packet is in response to the storing of the information. Nowhere in paragraph [0040] of Noehring et al. does Noehring et al. contemplate determining priority of the information flow or transferring the operated-on portion of the data from memory based on the priority of the information flow associated with the portion of the data as recited in the subject claim. Accordingly, this rejection should be withdrawn.

Claim 8, which depends from claim 1, recites that the processor includes, *inter alia*, logic configured to compress the portion of the data using the processor prior to

performing the security operations when the retrieved portion is non-secure data and logic configured to decompress the portion of the data in the processor after performing the security operations when the retrieved portion is secure data. **Claims 17 and 26** recite similar aspects.

The Office asserts that Noehring et al. teaches such claimed aspects at page 5, paragraph [0045], and page 8, paragraph [0078]. However, these sections of Noehring et al. do not teach or suggest the above claimed aspects. As noted by the Office, the referenced sections of Noehring et al. relate to encapsulation. In particular, page 5, paragraph [0045] states that "during pre-crypto packet processing, encapsulation headers 55 and 56 are added to the packet which are referred to as outer header 56 and IPSEC header 55." However, adding encapsulated headers is not the same as compressing data as recited in the subject claim.

During examination, the USPTO must give claims their broadest reasonable interpretation in light of the specification. (See MPEP §2111.01 *citing In re American Academy of Science Tech Center*, 367 F.3d 1359, 1369, (Fed. Cir. 2004)). The words of the claim must be given their plain meaning unless the plain meaning is inconsistent with the specification. (See MPEP §2111.01). As would be understood by one of ordinary skill in the art at the time of the invention, the plain meaning of encapsulation means to enclose in, as if in a capsule, whereas the plain meaning of compress refers to reducing in size, quantity, volume, etc. Moreover, the instant specification provides examples of compression algorithms and notes that in one example the compression can be lossless. (See Application, at least paragraphs [0043], [0063], [0069], [0072], [0073], [0076], [0077], and [0082]). Thus, rather than compressing the packets, Noehring et al. is doing the opposite; Noehring et al. is increasing the size by adding encapsulated headers.

In light of the above, this rejection should be withdrawn.

Amended independent **claim 12** recites, *inter alia*, retrieving a portion of the data from the memory into a processor using the memory controller, wherein portions of the data having higher priority information flow are retrieved before portions of the data having lower priority information flow. Noehring et al. is silent regarding priority information (as discussed *supra* with respect to claim 6), let alone retrieving portions of

the data having higher priority information flow before portions of the data having lower priority information flow. Accordingly, this rejection should be withdrawn.

Amended independent **claim 22** recites, *inter alia*, transferring the operated-on portion of the data from the memory to the network using the memory controller, wherein operated-on portions of the data having higher priority information flow are transferred before portions of the data having lower priority information flow. Noehring et al. is silent regarding priority information (as discussed *supra* with respect to claim 6), let alone transferring portions of the data having higher priority information flow before portions of the data having lower priority information flow. Accordingly, this rejection should be withdrawn.

Claims 2-5, 7, 9, 13, 14, 16, 20, 21, 23, and 24-16 directly or indirectly depend from independent claims 1, 12, and 22 and are allowable by virtue of their dependencies.

The Rejection of Claims 10, 11, 18, and 19 under 35 U.S.C. 103(a)

Claims 10, 11, 18, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Noehring et al. in view of Trost et al. **Claim 10, 11, 18, and 19** directly or indirectly depend from independent claims 1 and 12 and are allowable by virtue of their dependencies.

Conclusion

In view of the foregoing, it is submitted that the subject claims distinguish patentably and non-obviously over the prior art of record. An early indication of allowability is earnestly solicited.

Respectfully submitted,

Date: August 9, 2007 By: 

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